REMARKS

In view of the following remarks, Applicant respectfully requests reconsideration and allowance of the subject application. This amendment is believed to be fully responsive to all issues raised in the Office Action mailed January 5, 2004.

Drawing Amendments

Submitted herewith are formal drawings addressing all issued raised in the Office Action.

Specification Amendments

The specification has been amended to address the issued raised in the Office Action.

Claim Rejections

Rejections Under 35 U.S.C. §102

Claims 1-4 were rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,647,016 to Isoda, et al. (hereinafter, "the '016 patent"). Applicant respectfully traverses this rejection.

Initially, Applicant respectfully submits that the Action fails to establish a *prima facie* case that the '016 patent anticipates independent **claim 1**. Anticipation under 35 U.S.C. §102 requires that *each and every element* of the claim be set forth *in the manner recited in the claim* in a single prior art reference. (See, MPEP 2131). Independent claim 1 positively recites "[a]n initiator node *for a storage area network*, the node intended to be coupled over a *storage area network* to *at least one storage node* having command queue capability . . ." However, the Action sets forth no evidence or argument that the '016 patent discloses (or even suggests) that the initiator

node is for a storage area network, or that the initiator node is intended to be coupled over a storage area network to at least one storage node having command queue capability, as recited in claim 1. Therefore, the Action fails to establish a *prima facie* case of anticipation.

Applicant further submits that the '016 patent cannot anticipate (or render obvious) independent claim 1 because the '016 patent neither discloses (nor even suggests) limitations explicitly recited in independent claim 1.

Claim 1 explicitly recites that the memory system stores "instructions for initializing the maximum queue depth for the at least one storage node to a value dependent on a type of the at least one storage node." The Action asserts that the '016 patent discloses this limitation, and cites column 11, lines 49-59 and column 19, lines 54-56 to support the rejection. Applicant disagrees. The cited text reads as follows:

> The "seq_ID" (sequence ID) field 308 indicates a sequential identifier which is allocated every reference queue in forming order of the ORBS. In the embodiment, the identifier is given so as to increase each time the ORB is formed.
>
> After the "seq_ID" field increases to the maximum value, it is returned to "0" in the next increase. A counter which gives a value to the sequence ID field and serves as a reference is provided in a region where it is not influenced by the bus reset or another obstacle. This is because the processes are performed in the target while increase performance of the sequence ID is used as a prerequisite.

Nothing in this text discloses (or even suggests) that the initiator's memory system includes instructions for initializing the maximum queue

depth for the at least one storage node to a value dependent on a type of the at least one storage node, as explicitly recited in claim 1.

Claim 1 further recites that the memory system stores "instructions for limiting the number of commands queued to a storage node of the at least one storage node to the current queue depth associated with the storage node." The Action asserts that the '016 patent discloses this limitation, and cites column 3, lines 43-46 and column 3, line 65 to column 4, line 2 to support the rejection. Applicant disagrees. The cited text reads as follows:

> Since the initiator transmits commands to the target so as not to exceed the number of commands in each queue, there is a case where commands assured in the queues which are not used are in vain.
>
> Further another object of the invention is to provide communication control method and apparatus which can efficiently use resources by unitarily managing the number of commands which can be transmitted from an initiator to a target instead of managing it every queue of the target.

Nothing in this text discloses (or even suggests) that the initiator's memory system includes instructions for limiting the number of commands queued to a storage node of the at least one storage node to the current queue depth associated with the storage node, as explicitly recited in claim 1.

Claim 1 further recites that the memory system stores "instructions for dynamically adjusting the current queue depth associated with the storage node based upon queue refusals generated by the storage node and the maximum queue depth associated with the storage node." The Action asserts that the '016 patent discloses this limitation, and cites column 4, lines

3-12 to support the rejection. Applicant disagrees. The cited text reads as follows:

> Further another object of the invention is to provide communication control method and apparatus in which an initiator dynamically performs an allocation to all of command pool areas of a target in a multiplex path by queues, thereby improving communicating efficiency and resource using efficiency of the target, and the number of command pool areas of the target is increased or decreased in accordance with the number of queues which are used for connection, thereby improving the resource using efficiency of the target.

Nothing in this text discloses (or even suggests) that the initiator's memory system includes instructions for dynamically adjusting the current queue depth associated with the storage node based upon queue refusals generated by the storage node and the maximum queue depth associated with the storage node, as explicitly recited in claim 1.

In sum, the '016 patent fails to disclose (or event to suggest) each of the specific limitations associated with the memory system recited in claim 1. Therefore, the '016 patent cannot anticipate (or render obvious) independent claim 1.

Applicant notes that claims 2-3 depend from independent claim 1, and are allowable by virtue of their dependency. In addition, Applicant respectfully traverses the rejections of dependent claims 2-3.

Claim 2 recites that the memory system stores "instructions for adjusting the current queue depth associated with a storage node downwardly when the current queue depth is greater than a minimum queue depth and the storage node refuses to queue a command issued by the initiator node." The Action asserts that the '016 patent discloses this

limitation, and cites column 9, lines 42-51 to support the rejection. Applicant disagrees. The cited text reads as follows:

> The total number of areas in the prefetch pool is held by the equipment as a target. This value is read out from the target at the time of login or the like and stored into the initiator.
>
> The example in the diagram shows a state where the total number of areas in the prefetch pool is equal to "10". The number (in the current ORB list) in the Current-QUE counter associated with the I/O request queue is increased or decreased in accordance with the formation and deletion of the ORB.

Nothing in this text discloses (or even suggests) that the memory system stores instructions for adjusting the current queue depth associated with a storage node downwardly when the current queue depth is greater than a minimum queue depth *and the storage node refuses to queue a command issued by the initiator node*, as explicitly recited in claim 2.

Claim 2 further recites that the memory system stores instructions "for adjusting the current queue depth upwardly when the current queue depth is less than the maximum queue depth associated with the storage node and that storage node has not refused to queue any commands issued by the initiator node for a determined period of time." The Action asserts that the '016 patent discloses this limitation, and cites column 7, lines 7-9, column 9, lines 52-65, and column 10, lines 48-53 to support the rejection. Applicant disagrees. The cited text reads as follows:

> For example, the CPU 1 executes a developing (rasterizing) process of an outline font into a display information RAM set on the RAM 2, thereby enabling WYSIWYG on the CRT 10. The CPU 1 opens various registered windows on the basis of commands instructed by a mouse cursor or the like (not shown) on the CRT 10 and executes various data processes.

> Upon formation of the ORB, if the current value in the Current-QUE counter, namely, the number (in the current ORB list) of commands does not exceed the number of reserved areas in the prefetch pool allocated to the I/O request queues at the initial stage, the number in the Current-QUE counter is increased and the ORB is added into the ORB list. Otherwise, a check is made to see if the number in the Current-POOL counter is equal to or larger than "1". If it is equal to or larger than "1", the number in the Current-POOL counter is decreased, the number in the Current-QUE counter is increased, and the ORB is added into the ORB list. If the number in the Current-POOL counter is already equal to "0", the ORB is not added into the ORB list.
>
> The example in the diagram shows a state where four reference queues 105a, 105b, 105c, and 105d and a management reference queue 105f exist. The number of reference queues is not limited to 4. The reference queues are dynamically prepared when a communication of each client process is connected. One or a plurality of reference queues are used for communication of each client process.

Nothing in this text discloses (or even suggests) that the memory system stores instructions "for adjusting the current queue depth upwardly when the current queue depth is less than the maximum queue depth associated with the storage node *and that storage node has not refused to queue any commands* issued by the initiator node for a determined period of time, as explicitly recited in claim 2.

Claim 3 recites that the memory system stores "instructions for monitoring logins, and for adjusting the current queue depth downwardly when a login by an additional initiator node is recognized." The Action asserts that the '016 patent discloses this limitation, and cites column 9, lines 42-51 to support the rejection. Applicant disagrees. The cited text reads as follows:

> By the opening process of each of the initiator and the target in FIGS. 16 and 17, a

> request queue can be formed in the initiator, a reference queue can be formed in the target, and a path is set between them. The procedures of FIGS. 16 and 17 are also used upon setting of a management path (a pair of management request queue and management reference queue) which is formed at the time of login.
>
> After that, the status block in response to the disconnection command is returned (step S2804). At this time point, all of the un-processed pointers remaining in the reference queue are returned to the free reference list (step S2805). If the prefetch pool was increased upon connection, the added amount is decreased and the pointers in the free reference list which is referred to are deleted by the decreased amount. Further, the pointers or the like for the reference queues are also deleted (step S2806). The processing routine is returned.

Nothing in this text discloses (or even suggests) that the memory system stores instructions for monitoring logins, and for adjusting the current queue depth downwardly when a login by an additional initiator node is recognized, as explicitly recited in claim 3.

Applicant respectfully submits that the Action fails to establish a *prima facie* case that the '016 patent anticipates independent **claim 4**. Claim 4 was summarily rejected, and the Action asserts that the subject matter of claim 4 is the same as that of claims 1-3. However, a close inspection of independent claim 4 reveals that the limitations of claim 4 are not identical to those of claims 1-3. The Action sets forth no evidence or argument that the '016 patent discloses (or even suggests) the specific limitations recited in claim 4. With respect, the Examiner is reminded that each and every element as set forth in a claim must be present in a cited reference for anticipation to be established under 35 USC §102; it is impermissible to consider a claim based on an assumed "gist" or generalized "subject matter"

of the claimed invention. Therefore, the Action fails to establish a *prima facie* case of anticipation of claim 4.

Applicant notes with appreciation the indication that **claims 5-9** are allowable.

CONCLUSION

Claims 1-9 are believed to be in condition for allowance. Applicant respectfully requests reconsideration and prompt issuance of the present application. Should any issue remain that prevents immediate issuance of the application, the Examiner is encouraged to contact the undersigned attorney to discuss the unresolved issue.

Respectfully Submitted,
Jed W. Caven

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Jed W. Caven
Lee & Hayes, LLP
Reg. No. 40,551
(303) 539-0265 x 246

Direct correspondence to:
Hewlett-Packard Company
Intelletual Property Administration
P.O. Box 272400
Fort Collins, CO 80527-2400